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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,594	08/19/2003	Nobuyasu Kanekawa	056207.50307C1	2784
23911	7590	05/05/2004	EXAMINER	
CROWELL & MORING LLP INTELLECTUAL PROPERTY GROUP P.O. BOX 14300 WASHINGTON, DC 20044-4300			DICKEY, THOMAS L	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicant(s)

10/642,594

Applicant(s)

KANEKAWA ET AL.

Examiner

Thomas L Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 15-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 09/943,384.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 08/19/2003.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

1. The preliminary amendments filed on 08/19/2003 and 09/22/2003 have been entered.

### ***Oath/Declaration***

2. The oath/declaration filed on 08/19/2003 is acceptable.

### ***Drawings***

3. The formal drawings filed on 08/19/2003 are acceptable.

### ***Priority***

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/943,384, filed on 08/31/2001.

### ***Information Disclosure Statement***

5. The Information Disclosure Statement filed on 08/19/2003 has been considered.

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***Specification***

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 15 and 18 are rejected under 35 U.S.C. § 102(b) as being anticipated by YUKUTAKE et al. (WO 9844687 A1).

Yukutake et al. discloses a semiconductor device, comprising an embedded insulation layer 232 formed in a semiconductor substrate 231; a plurality of power semiconductor elements 215-216-218 formed on said semiconductor substrate 231; a trench 206-1 through 206-6 isolating between said plurality of power semiconductor elements 215-216-218 formed on said semiconductor substrate 231 on said embedded insulation layer 232; an isolator 207 insulating and driving control electrodes of said power semiconductor elements 215-216-218; and wherein said plurality of power semiconductor elements 215-216-218 are each connected to multiple device terminals in order to provide connectability to said semiconductor device, wherein said plurality of

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power semiconductor elements 215-216-218 have an input control circuit 213-214-217 supplying a control signal of a specific control pattern to said control electrodes of said plurality of power semiconductor elements 215-216-218 on the base of input signals.

Note, for example, figures 8a and 8b of Yukutake et al.

**B.** Claim 15 is rejected under 35 U.S.C. § 102(b) as being anticipated by NEMOTO et al. (WO 9966557 A1).

Nemoto et al. discloses a semiconductor device, comprising an embedded insulation layer 10 formed in a semiconductor substrate 11; a plurality of power semiconductor elements (MOSFETS, not shown but described at page 7 lines 25-27) formed on said semiconductor substrate 11; a trench 6e isolating between said plurality of power semiconductor elements formed on said semiconductor substrate 11 on said embedded insulation layer 10; an isolator 4 insulating and driving control electrodes (not shown, see page 7 lines 25-27 for the description of the MOSFETS containing the control electrodes) of said power semiconductor elements; and wherein said plurality of power semiconductor elements are each connected to multiple device terminals 5b in order to provide connectability to said semiconductor device. Note figures 1-4 and page 7 lines 25-27 of Nemoto et al.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**A. Claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over NEMOTO ET AL. (WO 9966557 A1) in view of MIURA (4,993,396).**

Nemoto et al. discloses a semiconductor device with all the limitations of claim 16 except an ignition coil driven by the power semiconductor elements. Note figures 1-4 and page 7 lines 25-27 of Nemoto et al.

However, Miura discloses a semiconductor device with an ignition coil 2 driven by power semiconductor element 1. Note figure 1 and column 4 lines 27-46 of Miura. Therefore, it would have been obvious to a person having skill in the art to use the power semiconductor elements of Nemoto et al.'s semiconductor device to drive an ignition coil such as taught by Miura because power semiconductor elements have a faster rise time and generate higher voltages into inductive loads such as ignition coils.

**B. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over NEMOTO et al. (WO 9966557 A1) in view of FOERSTER (5,828,141).**

Nemoto et al. discloses a semiconductor device with all the limitations of claim 16 except a fuel injector driven by the power semiconductor elements. Note figures 1-4 and page 7 lines 25-27 of Nemoto et al.

However, Foerster discloses a semiconductor device with a fuel injector driven by power semiconductor elements. Note figure 1 and column 1 lines 32-35 of Foerster. Therefore, it would have been obvious to a person having skill in the art to having skill in

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the art to use the power semiconductor elements of Nemoto et al.'s semiconductor device with the fuel injector driven by power semiconductor elements such as taught by Foerster in order to demagnetize the inductive load presented by the fuel injector as rapidly as possible, in a repeatable fashion.

### ***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**TLD**  
**03/2004**

  
**Minhloan Tran**  
**Primary Examiner**  
**Art Unit 2826**